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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647;687	08/25/2003	S. Brandon Keller	100111228-1	2951

22879 7590 10/04/2005

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,687	KELLER ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/25/03, 2/6/04, 1/20/05 and 6/8/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04, 1/20&6/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

- Page 1, paragraph 0001: the Serial Numbers of the Copending, cofiled U.S. Patent Applications are missing.
- Page 7, paragraph 0028, second line: The Figure number of the first occurrence of "FIG." is missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 – 7 and 9 - 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,831,869 to Ellis et al. (hereinafter, "Ellis").

3. Referring to claims 1, 7, 16 and 17, Ellis teaches a method (claim 1), a system (claims 7 and 16) and a computer program (claim 17) for utilizing fast analysis information during detailed analysis of a circuit (see col. 3, lines 33 – 57; Fig. 2) comprising: electronically analyzing design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the blocks

(see Figs. 3 and 13; col. 4, lines 1 – 27; col. 11, line 62 – col. 12, line 18); determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions (see Figs. 10,11, 14 and 17; col. 12, lines 19 – 48; col. 13, lines 51 – 62) and; if the hierarchical signal net connectivity matches the assumptions utilizing the fast analysis results to generate detailed analysis results, and if it does not, analyzing the blocks to generate detailed analysis results (see also Figs. 4 and 5; Abstract, col. 7, line 17 – col. 9, line 29). Thus, Ellis clearly discloses all the claimed limitations.

4. As per claims 3 and 9, see Figs. 8 and 9, which show that the ported signal nets are not connected to power nets, as claimed.

5. Pursuant to claims 4, 10 and 18, see Figs. 8, 9 and 12, which cite the claimed elements pertaining to FET connections in the blocks.

6. Regarding claims 5, 11 and 19, see (3) above, and particularly Fig. 5; col. 8, line 19 - col. 9, line 29, which teach the claimed elements pertaining to the assumptions utilized in determining fast analysis results.

7. As for claims 6, 12 and 20, see Figs. 10 – 17 which all disclose reading instantiation characteristics to determine block instances, as claimed.

8. Referring to claims 13, 14 and 15, see Fig. 2, block 32; col. 6, lines 8 – 45, which cite how the claimed databases can be generated and stored.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis in view of Publication No. US 2002/0002701 A1 to Usami et al. (hereinafter, "Usami").

11. Pursuant to claims 2 and 8, the teachings of Ellis with regards to a method and system for utilizing fast analysis information during detailed analysis of a circuit design are recited above, and described in detail in his disclosure. However, Ellis is silent on the inclusion of FET leakage current in his fast and detailed analysis results, as claimed. However, Usami cites an automatic circuit generation methods and apparatus for analyzing a circuit for leakage currents, and also provides a way of eliminating or reducing the leakage currents (see Usami – Figs. 3 and 10; page 1, paragraphs 0003 and 0005). Since, as cited by Usami (paragraph 0005), leakage currents can cause a serious problem in VLSI circuits, and can decrease the battery life in battery drivers

such as cell phones, lap-top computers, etc, it would therefore be obvious to a person of ordinary skill in the art at the time of the invention to combine the teachings of Ellis and Usami to obtain the same claimed invention.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No. US 2004/0044972 A1 to Rohrbaugh et al. cites a method and apparatus of carrying out a computer – assisted analysis function on a hierarchical circuit model by inputting the hierarchical model, specifying at least one circuit block within the hierarchy as a target, and simplifying the hierarchical model by deleting circuit blocks not affecting the analysis function to produce a simplified model.

Pub. No. US 2004/0078767 A1 to Burks et al. discloses a method for modeling IC designs in a hierarchical design automation system which utilizes a block abstraction that are necessary to achieve accurate placement, routing, extraction, simulation, and verification of the block's ancestors in the hierarchy.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
28 September 2005

MYD

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800